# XC61C Series Voltage Detectors

# Application Notes

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| WARNING |
| --- |
| As the voltage detector depends on not only the IC's characteristics but also on those of the surrounding circuitry, please fully ensure that the 'notes on use' provided are followed.<br>In actual operation we suggest that you allow ample margins above the recommended specifications and take the IC's and the peripheral's absolute maximum ratings into consideration. |

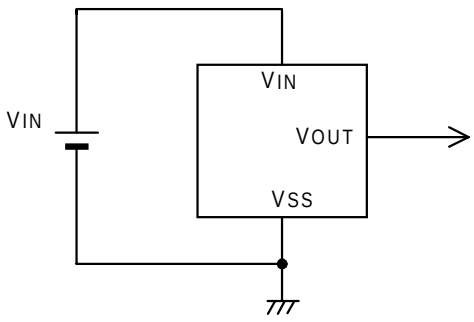
## ❍ Introduction

The XC61C series are highly accurate, low power consumption voltage detectors manufactured using laser trimming and CMOS process technologies. The series consists of an output driver circuit, a hysteresis circuit, a comparator and a highly accurate standard voltage supply.

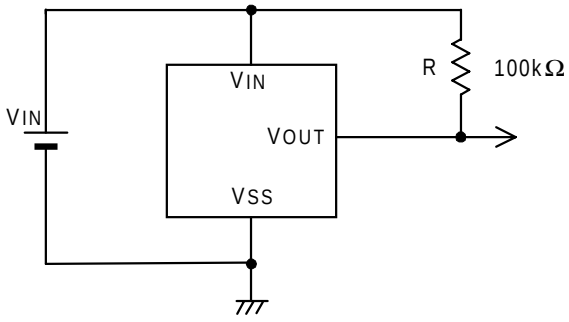
Detect voltage has minimal temperature drift. Both CMOS and N-channel open drain output configurations are available.

All the above functions are provided in a super mini-mold package that supports high density mounting.

## ❍ Standard Circuits




CMOS Configuration




Nch Open Drain Configuration

## ❍ Notes on Use

**1. Oscillation as a result of output current with CMOS output configurations**

As oscillation may occur due to load current ($I_{OUT}$) with CMOS output configurations if anything which acts like a resistor is present between the $V_{IN}$ pin and the power supply, we recommend that you use Nch open drain output configurations where $R_{IN}$ is used.

**N.B.**

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current ($I_{OUT}$) will flow through $R_L$. Because a voltage drop ($R_{IN}$ x $I_{OUT}$) is produced at the $R_{IN}$ resistor, located between the input (IN) and the $V_{IN}$ pin, the load current will flow via the IC's $V_{IN}$ pin. The voltage drop will also lead to a fall in the voltage level at the $V_{IN}$ pin.

When the $V_{IN}$ pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at $R_{IN}$ will disappear, the voltage level at the $V_{IN}$ pin will rise and release operations will begin over again.

Oscillation may occur with this " release – detect – release" repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

Note : Do not use $R_{IN}$ with CMOS output configurations as oscillation may occur.

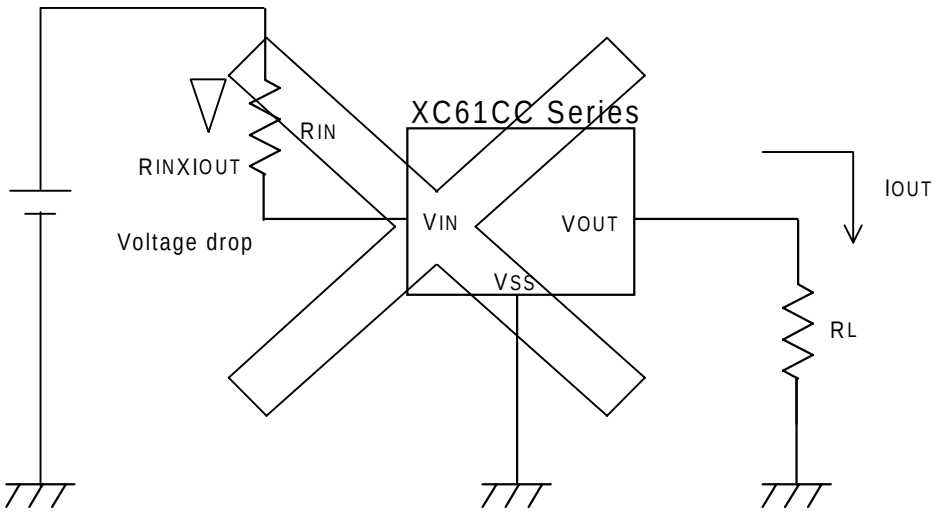



Diagram 1. Oscillation resulting from output current

**2. Oscillation as a result of through current**

Please note that if a resistor is connected between the VIN pin and the power supply with CMOS output configurations (irrespective of N-channel output configurations), oscillation may occur as a result of through current at the time of voltage release.
(Please refer to Diagram 2)
Through current is the current that flows excessively when the IC's internal circuit voltage level changes (during release and detect operations).

**N.B.**

When the voltage applied at IN rises, release operations commence, the detector's output voltage increases and through current flows. Because a voltage drop (RIN x ISS) is produced at the RIN resistor, located between the input (IN) and the VIN pin, this through current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin.
When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, through current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.
Oscillation may occur with this " release – detect – release" repetition.
However, since hysteresis exists during detect operations, oscillation is unlikely to occur. In comparison to N-channel output configurations, through current in the final stages is larger with CMOS output configurations, which tends to result in oscillation occurring somewhat more easily.

Note : Do not use RIN with CMOS output configurations as oscillation may occur.

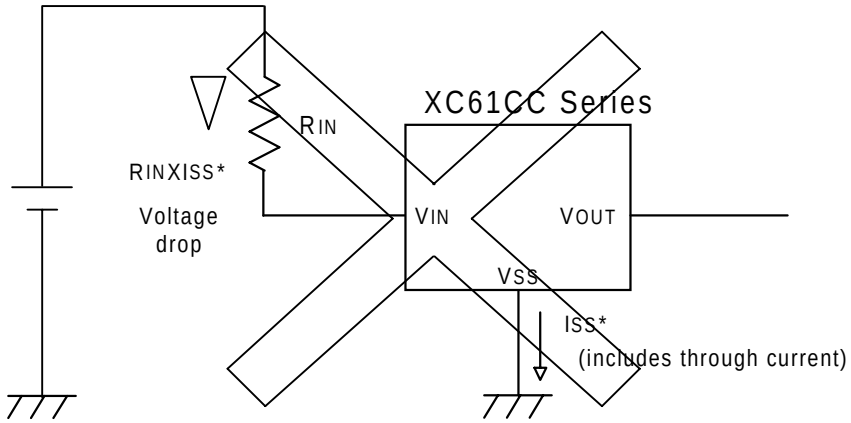
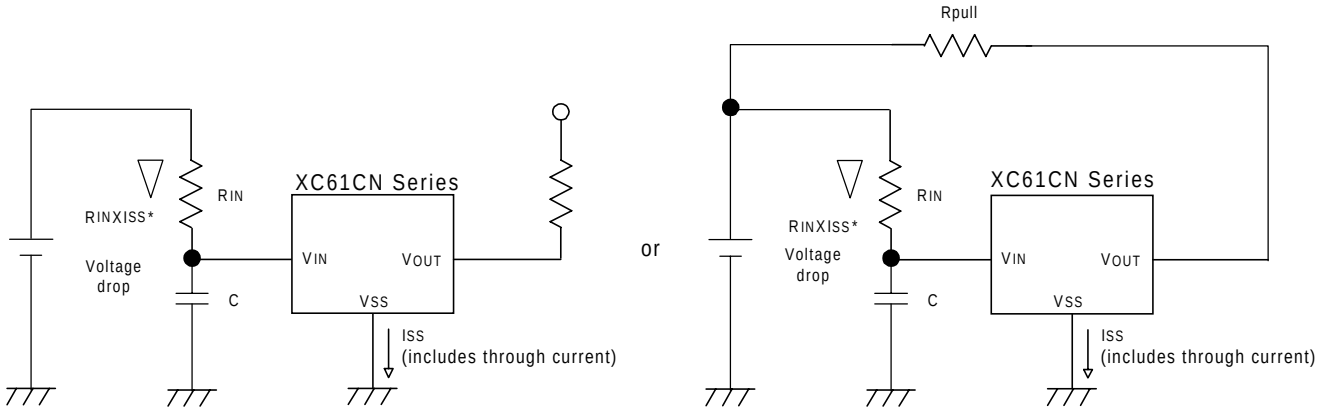



Diagram 2. Oscillation resulting from through current

Always use the N-channel open drain output configuration if an input resistor (RIN) is to be used and/or the input voltage is to be divided. (Please refer to Diagram 3 )
With an input resistor (RIN) present, release voltage will rise if a pull up resistor (Rpull) is connected between the VIN – VOUT pins and input voltage is divided between RIN and Rpull. It is therefore recommended that the pull up resistor be connected to the power supply side. (Please refer to Application Circuits 3, page 11)




* Pull up resistor connected to separate power supply

* Pull up resistor connected to input

Diagram 3. Example circuit with Input Resistor connected

N.B. Please ensure that RIN = less than 10kΩ, C = more than 0.1μF

Please be aware that both detect and release voltages will rise due to voltage drops at RIN brought about by the IC's supply current.

**3. Operational errors resulting from steep frequency inputs**

Should steep start up voltages be input at the VIN pin, frequencies output from VOUT may become distorted so please regulate input frequency start up time (MIN) to a standard of more than several μ seconds/V.

**4. Power Dissipation Pd**

Please observe the following points :

CMOS

(VIN – VOUT) x IOUT < Pd : Release time (PchFET : ON)

VOUT x IOUT < Pd : Detect time (NchFET : ON)

Should output ($V_{OUT}$) short to ground during release operations, the resulting heat from the loss at $V_{IN}$ x $I_{OUT}$ may cause damage to the IC so please take all necessary precautions.

N-channel open drain

$V_{OUT}$ x $I_{OUT}$ < Pd : Detect time

**5. Pull up resistor with N-channel open drain configurations**

If the pull up resistance value is extremely large, output voltage may drop during release operations as a result of the N-channel transistor leak current within the IC.
It is therefore recommended that a pull up resistance of less than 470kΩ be used.
(a pull up resistor is not necessary with CMOS output configurations)

## ❍ Application Circuits

### 1. Power ON reset circuit

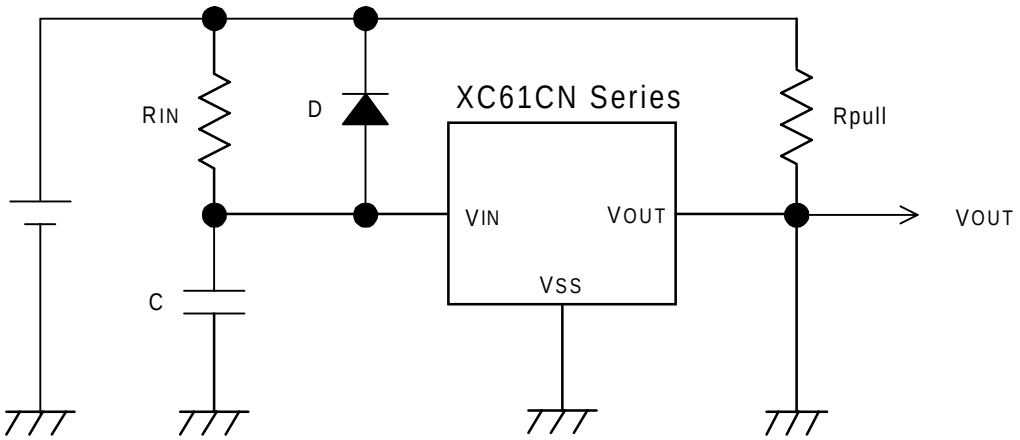



Diagram. Power ON reset circuit

XC61CN series

Peripherals :

RIN : 10kΩ

C : 3.3μF

Ex.) When input voltage rises from 0V to 4V,
delay time tDLY = 46msec (VDR = 3.0V)
(Please refer to the notes on tDLY below)

D : 1S1588

Rpull : 100kΩ

Notes on Use :

It is recommended that RIN = less than 10kΩ and that C = more than 0.1μF in order to avoid oscillation.

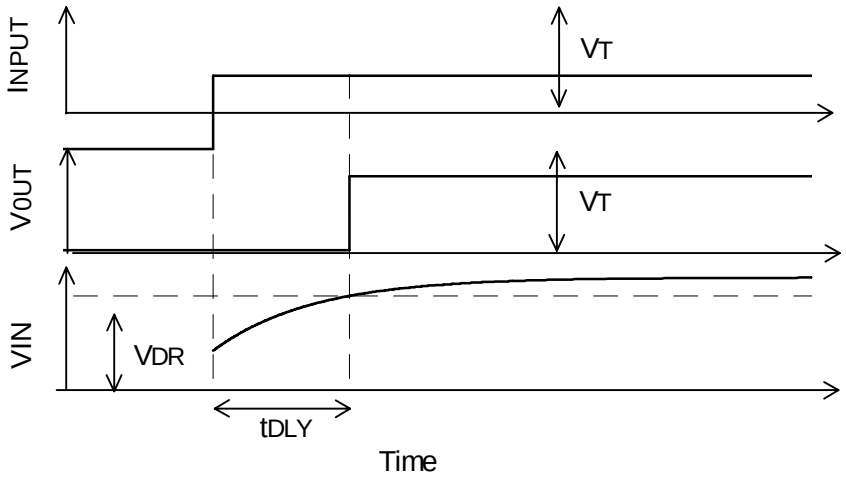
Note that the above does not apply to CMOS output (XC61CC series) configurations. (Please refer to ‘Notes on Use 1’, page 3)

If pull up is connected to the input, please ensure that the settings for VOUT are not exceeded.

Notes :

1. The value for delay time tDLY can be calculated as follows :
   tDLY = – RIN・C・In (1-VDR/VT) (sec)
   where VT = Input voltage peak value, VDR = Release voltage

2. Output waveforms when power is switched on :




Explanation :

A power ON reset circuit can be realized by using the N-channel open drain configuration. Delay time during start up is regulated via the external input resistor ($R_{IN}$) and capacitor (C).

When power is switched off the electric charge that had charged C is discharged by the diode (D).

## ❍ Application Circuits

### 2. High voltage detection circuit

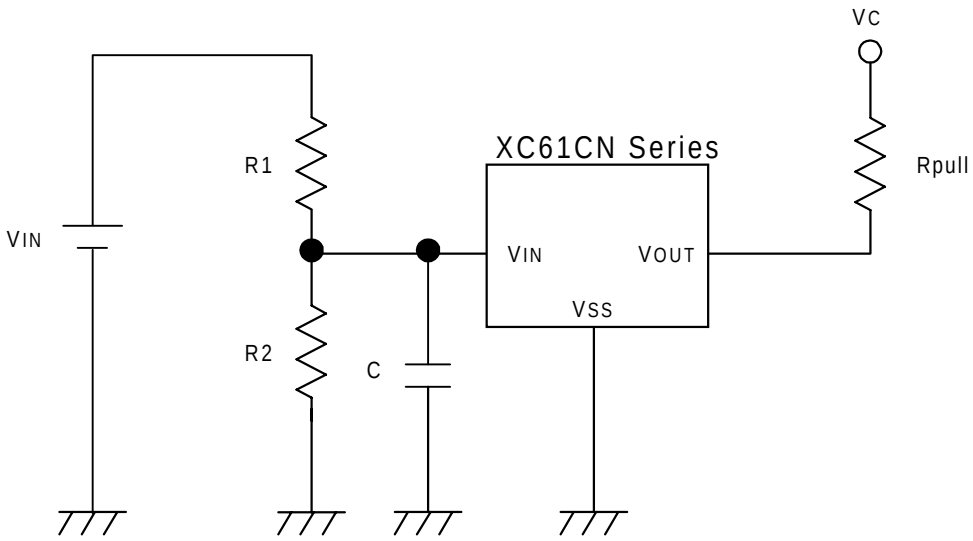



Diagram. High voltage detection circuit

XC61CN series

Peripherals :

R1 : 10kΩ

R2 : 5kΩ

Ex.) Detect voltage $V_{DF}$ = 3.0V

Set-up detect voltage $V_{DH}$ = 9.0V

Hysteresis range increases from 0.15V(typ) to 0.45V

(Please refer to the notes on detect voltage $V_{DH}$ and hysteresis range $V_{HYSH}$ provided below)

C : 0.1μF

Rpull : 100kΩ

Notes on Use :

It is recommended that R1 = less than 10kΩ and that C = more than 0.1μF in order to avoid oscillation.

Note that the above does not apply to CMOS output (XC61CC series) configurations.

Notes :

The value for detect voltage $V_{DH}$ and hysteresis range $V_{HYSH}$ can be calculated as follows :

$V_{DH} = V_{DF} \cdot (R_1 + R_2) \div R_2$ (V)

$V_{HYSH} = V_{HYS} \cdot (R_1 + R_2) \div R_2$ (V)

where $V_{DF}$ = the IC's detect voltage value

$V_{DH}$ = the actual circuit's detect voltage value

$V_{HYS}$ = the IC's hysteresis range

$V_{HYSH}$ = the actual circuit's hysteresis range

Please note that due to the IC's supply current $I_{SS}$, $V_{DH}$ will be higher than, and $V_{HYSH}$ will be larger than, the calculated values.

Explanation :

Should the required voltage detector be unavailable, it is possible to achieve a detect voltage higher than the IC's established value by using divided resistors, but only with N- channel open drain output configurations.

## ❍ Application Circuits

### 3. Hysteresis range enlargement circuit

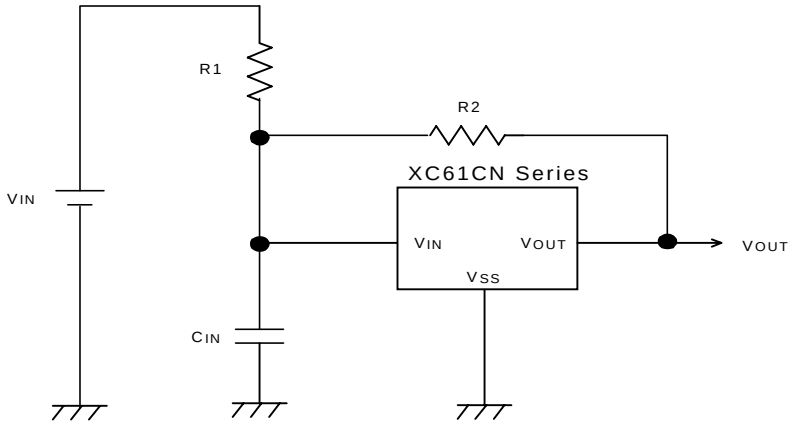



Diagram. Hysteresis range enlargement

XC61CN series

Peripherals :

$R_1$ : 3kΩ

$R_2$ : 33kΩ

$C_{IN}$ : 0.1μF

Ex.) Release voltage $V_{DR}$ = 3.15V, $R_1$=3kΩ, $R_2$=33kΩ

Set-up release voltage $V_{DR1}$ = 3.44V

Release voltage therefore increases by 0.29V

(Please refer to the notes on release voltage provided below)

Notes :

The value for release voltage $V_{DR1}$ can be calculated as follows :

$$V_{DR1} = V_{DR} \cdot (R_1 + R_2) \div R_2$$

where $V_{DR}$ = the IC's release voltage value

$V_{DR1}$ = the actual circuit's release voltage value

Please note that due to the IC's supply current $I_{SS}$, $V_{DR1}$ will be higher than the calculated values.

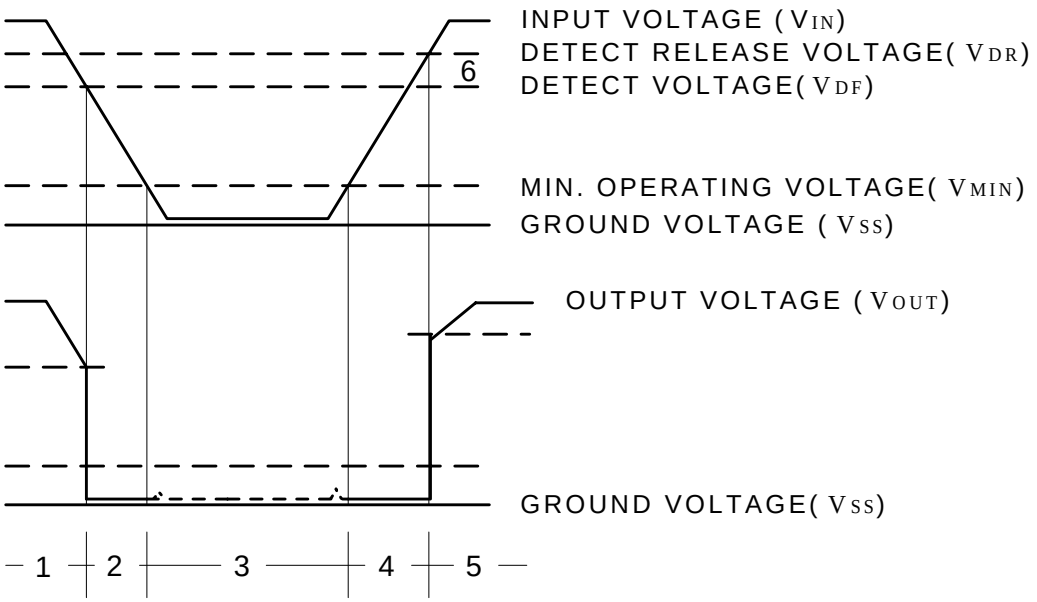
Explanation :

With N- channel open drain output configurations it is possible to enlarge the hysteresis range without having to change detect voltage.

N.B. Please use with a value for $R_1$ below 10kΩ

## ❍ Appendix

### Time Chart




**Functional Explanation (CMOS output)**

1. When input voltage (VIN) rises above detect voltage (VDF), output voltage (VOUT) will be equal to VIN.
   Note that as a condition of high impedance exists at the VOUT pin with N-channel open drain configurations, pull up voltage can be obtained via pull up resistance.
2. When VIN falls below VDF, VOUT will equal ground voltage (VSS).
3. When VIN falls to a level below that of the minimum operating voltage (VMIN), output becomes unstable.
   Note that as the output pin is generally pulled up with N-channel open drain output configurations, output will be equal to pull up voltage.
4. When VIN rises above the VSS level, output will be unstable at levels below VMIN. Between the VMIN and detect release voltage (VDR) levels, the VSS level will be maintained.
5. When VIN rises above VDR, VOUT will be equal to VIN.
   Note that a condition of high impedance exists with N-channel open drain Configurations (refer to explanation 1).
6. The difference between VDR and VDF represents the hysteresis range (VHYS).